

---

# PXle-7890

# Specifications

---

2025-09-25



# Contents

PXIe-7890 Specifications ..... 3

# PXIe-7890 Specifications

## PXIe-7890 Specifications

These specifications apply to the PXIe-7890.

## Looking For Something Else?

For information not found in the specifications for your product, such as operating instructions, browse ***Related Information***.

### Related information:

- [PXIe-7890/7891 Getting Started](#)
- [Software and Driver Downloads](#)
- [Dimensional Drawings](#)
- [Product Certifications](#)
- [Letter of Volatility](#)
- [Discussion Forums](#)
- [NI Learning Center](#)

## Definitions

***Warranted*** specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

***Characteristics*** describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- ***Typical*** specifications describe the performance met by a majority of models.
- ***Nominal*** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- ***Measured*** specifications describe the measured performance of a representative model.

Specifications are **Typical** unless otherwise noted.

## Conditions

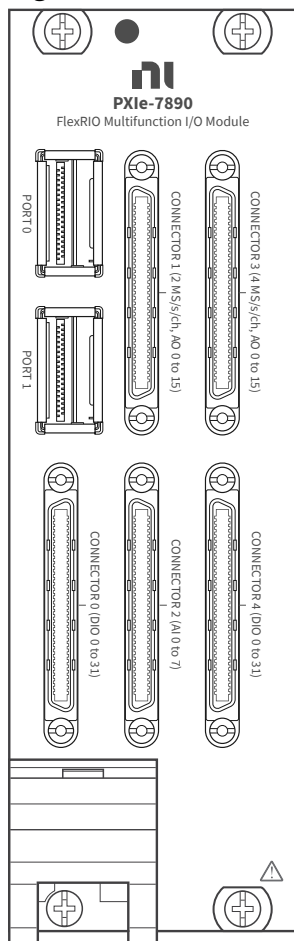
Specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature of 0 °C to 55 °C .
- Installed in chassis with slot cooling capacity  $\geq 58$  W.

## Front Panel

The following image shows the front panel of the PXIe-7890 module. This document groups specifications per connector on the front panel.

Figure 1. PXIe-7890 Front Panel



# Connector Pinouts

## PORT 0 and PORT 1

The following image shows the pinout for the PORT 0 and PORT 1 QSFP connectors.

Figure 2. QSFP Connector Pinout

GND	20	19	GND
Rx2n	21	18	Rx1n
Rx2p	22	17	Rx1p
GND	23	16	GND
Rx4n	24	15	Rx3n
Rx4p	25	14	Rx3p
GND	26	13	GND
ModPrsL	27	12	SDA
IntL	28	11	SCL
Vcc Tx	29	10	Vcc Rx
Vcc1	30	9	ResetL
LPMODE	31	8	ModSelL
GND	32	7	GND
Tx3p	33	6	Tx4p
Tx3n	34	5	Rx4n
GND	35	4	GND
Tx1p	36	3	Tx2p
Tx1n	37	2	Tx2n
GND	38	1	GND

Table 1. Pin Descriptions for PORT 0 and PORT 1 Connectors

Pin	Description
Txn <1..4>	Transmitter Inverted Data Input
Txp <1..4>	Transmitter Non-Inverted Data Input
Rxn <1..4>	Receiver Inverted Data Output
Rxp <1..4>	Receiver Non-Inverted Data Output
SCL	2-Wire Serial Interface Clock
SDA	2-Wire Serial Interface Data
ModPrsL	Module Present

Pin	Description
ModSelL	Module Select
ResetL	Module Reset
IntL	Interrupt
LPMode	Low Power Mode
Vcc Rx	+3.3 V Power Supply Receiver
Vcc Tx	+3.3 V Power Supply Transmitter
Vcc1	+3.3 V Power Supply
GND	Ground

**!** **Notice** The maximum input signal levels are valid only when the module is powered on. To avoid permanent damage to the PXIe-7890/7891, do not apply a signal to the device when the module is powered down.

**!** **Notice** Connections that exceed any of the maximum ratings of any connector on the PXIe-7890/7891 can damage the device and the system. NI is not liable for any damage resulting from such connections.

## CONNECTOR 0 and CONNECTOR 4

The following image shows the pinouts for CONNECTOR 0 and CONNECTOR 4.

Figure 3. Digital I/O (DIO) Connectors

Connector 0			Connector 4				
GND	68	34	GND	DIO31	1	35	DIO30
EXTCLKIN	67	33	GND	GND	2	36	GND
GND	66	32	GND	DIO29	3	37	DIO28
DIO0	65	31	DIO1	GND	4	38	GND
GND	64	30	GND	DIO27	5	39	DIO26
DIO2	63	29	DIO3	GND	6	40	GND
GND	62	28	GND	DIO25	7	41	DIO24
DIO4	61	27	DIO5	GND	8	42	GND
GND	60	26	GND	DIO23	9	43	DIO22
DIO6	59	25	DIO7	GND	10	44	GND
GND	58	24	GND	DIO21	11	45	DIO20
DIO8	57	23	DIO9	GND	12	46	GND
GND	56	22	GND	DIO19	13	47	DIO18
DIO10	55	21	DIO11	GND	14	48	GND
GND	54	20	GND	DIO17	15	49	DIO16
DIO12	53	19	DIO13	GND	16	50	GND
GND	52	18	GND	DIO15	17	51	DIO14
DIO14	51	17	DIO15	GND	18	52	GND
GND	50	16	GND	DIO13	19	53	DIO12
DIO16	49	15	DIO17	GND	20	54	GND
GND	48	14	GND	DIO11	21	55	DIO10
DIO18	47	13	DIO19	GND	22	56	GND
GND	46	12	GND	DIO9	23	57	DIO8
DIO20	45	11	DIO21	GND	24	58	GND
GND	44	10	GND	DIO7	25	59	DIO6
DIO22	43	9	DIO23	GND	26	60	GND
GND	42	8	GND	DIO5	27	61	DIO4
DIO24	41	7	DIO25	GND	28	62	GND
GND	40	6	GND	DIO3	29	63	DIO2
DIO26	39	5	DIO27	GND	30	64	GND
GND	38	4	GND	DIO1	31	65	DIO0
DIO28	37	3	DIO29	GND	32	66	GND
GND	36	2	GND	GND	33	67	EXTCLKIN
DIO30	35	1	DIO31	GND	34	68	GND

Table 2. Pin Descriptions for CONNECTOR 0 and CONNECTOR 4

Pin	Description	Signal Name in LabVIEW
DIO <0..31>	Bidirectional digital input/output signal connection	Digital Input: <ul style="list-style-type: none"> <li>Conn0 DI / Ch &lt;0..31&gt;</li> <li>Conn4 DI / Ch &lt;0..31&gt;</li> </ul> Digital Output:

Pin	Description	Signal Name in LabVIEW
		<ul style="list-style-type: none"> <li>• Conn0 DO / Ch &lt;0..31&gt;</li> <li>• Conn4 DO / Ch &lt;0..31&gt;</li> </ul>
EXTCLKIN	External clock input source that can be used for source synchronous acquisitions; the provided clock source must be stable and glitch free	Conn 0 External Clock Conn 4 External Clock
GND	Ground reference for digital signals	—
NC	No connection	—

## CONNECTOR 1 and CONNECTOR 3

The following image shows the pinout for CONNECTOR 1 and CONNECTOR 3.

Figure 4. Analog Output (AO) Connectors

NC	1	35	NC
GND	2	36	GND
NC	3	37	NC
GND	4	38	GND
NC	5	39	NC
GND	6	40	GND
NC	7	41	NC
GND	8	42	GND
NC	9	43	NC
GND	10	44	GND
NC	11	45	NC
GND	12	46	GND
NC	13	47	NC
GND	14	48	GND
NC	15	49	NC
GND	16	50	GND
AO15	17	51	AO14
GND	18	52	GND
AO13	19	53	AO12
GND	20	54	GND
AO11	21	55	AO10
GND	22	56	GND
AO9	23	57	AO8
GND	24	58	GND
AO7	25	59	AO6
GND	26	60	GND
AO5	27	61	AO4
GND	28	62	GND
AO3	29	63	AO2
GND	30	64	GND
AO1	31	65	AO0
GND	32	66	GND
NC	33	67	NC
GND	34	68	GND

Table 3. Pin Descriptions for CONNECTOR 1 and CONNECTOR 3

Pin	Description	Signal Name in LabVIEW
AO <0..15> (PXle-7890) AO <0..31> (PXle-7891)	Analog output signal connection	PXle-7890: <ul style="list-style-type: none"> <li>• Calibrated: Conn1 AO / Ch &lt;0..15&gt;</li> <li>• Calibrated: Conn3 AO / Ch &lt;0..15&gt;</li> <li>• Uncalibrated: Conn1 AO Raw / Ch &lt;0..15&gt;</li> </ul>

Pin	Description	Signal Name in LabVIEW
		<ul style="list-style-type: none"> <li>Uncalibrated: Conn3 AO Raw / Ch &lt;0..15&gt;</li> </ul> PXIe-7891: <ul style="list-style-type: none"> <li>Calibrated: Conn1 AO / Ch &lt;0..31&gt;</li> <li>Calibrated: Conn3 AO / Ch &lt;0..31&gt;</li> <li>Uncalibrated: Conn1 AO Raw / Ch &lt;0..31&gt;</li> <li>Uncalibrated: Conn3 AO Raw / Ch &lt;0..31&gt;</li> </ul>
GND	Ground reference for the analog output signal	—
NC	No Connection	—

## CONNECTOR 2

The following image shows the pinout for CONNECTOR 2, the analog input VHDCI front panel connector.

Figure 5. Analog Input (AI) VHDCI Connector

GND	1	35	GND
AI0+	2	36	GND
AI0-	3	37	AI1+
GND	4	38	AI1-
AI2+	5	39	GND
AI2-	6	40	AI3+
GND	7	41	AI3-
AI4+	8	42	GND
AI4-	9	43	AI5+
GND	10	44	AI5-
AI6+	11	45	GND
AI6-	12	46	AI7+
GND	13	47	AI7-
NC	14	48	GND
NC	15	49	NC
GND	16	50	NC
NC	17	51	GND
NC	18	52	NC
GND	19	53	NC
NC	20	54	GND
NC	21	55	NC
GND	22	56	NC
NC	23	57	GND
NC	24	58	NC
GND	25	59	NC
GND	26	60	GND
GND	27	61	GND
GND	28	62	GND
GND	29	63	GND
GND	30	64	GND
GND	31	65	GND
GND	32	66	GND
GND	33	67	GND
GND	34	68	GND

Table 4. Pin Descriptions for CONNECTOR 2

Pin	Description	Signal Name in LabVIEW
AI <0+...7+> (PXIe-7890) AI <0+...15+> (PXIe-7891)	Positive analog input signal connection	PXIe-7890: <ul style="list-style-type: none"><li>• Calibrated: Conn2 AI / Ch &lt;0..7&gt;</li><li>• Uncalibrated: Conn2 AI / Ch &lt;0..7&gt;</li></ul>
AI <0-...7-> (PXIe-7890) AI <0-...15-> (PXIe-7891)	Negative analog input signal connection	PXIe-7891:

Pin	Description	Signal Name in LabVIEW
		<ul style="list-style-type: none"> <li>• Calibrated: Conn2 AI / Ch &lt;0..15&gt;</li> <li>• Uncalibrated:Conn2 AI / Ch &lt;0..15&gt;</li> </ul>
GND	Ground reference for the analog input signal	—
NC	No connection	—

## Port 0 and Port 1

Connector	QSFP, SFF-8436 compliant
Data rate	500 Mbps to 5 Gb/s
Number of lanes	8 RX/TX (GTH)
Supported high-speed cable type	Electrical/ optical
Optical cable power	3.3 V $\pm$ 5%, 1 A per port

## Multi-Gigabit Transceiver (MGT)

### MGT TX $\pm$ Channels



**Note** For detailed FPGA and High-Speed Serial Link specifications, refer to Xilinx documentation.

Minimum differential output voltage <sup>1</sup>	170 mV pk-pk into 100 $\Omega$ , nominal
I/O coupling	AC-coupled, includes 100 nF capacitor

## MGT RX± Channels

Differential input voltage range at $\leq 6.6$ Gb/s	150 mV pk-pk to 2000 mV pk-pk , nominal
---	---

## MGT Reference Clock Generator

Supported generated frequencies	60.000 MHz to 385.714 MHz 400.000 MHz to 450.000 MHz 480.000 MHz to 675.000 MHz 685.714 MHz to 771.428 MHz 800 MHz
Clocking resources	PXIe_CLK100
Available MGT Reference Clocks	4

## Connector 0 and Connector 4

The following section describes the digital input and output characteristics accessible through CONNECTOR 0 and CONNECTOR 4.

1. 800 mV pk-pk when transmitter output swing is set to the maximum setting.

CONNECTOR 0 and CONNECTOR 4 are identical and share the same pinout, but are oriented in opposite directions on the module. For more information, refer to the ***PXIe-7890/7891 Getting Started***.

Connectors 0 and 4	68-pin VHDCI receptacle
--------------------	-------------------------



**Note** The number of channels listed in each of the following sections represents the total number of channels for both CONNECTOR 0 and CONNECTOR 4. To determine the number of channels for a single connector, divide the listed number of channels in half.

#### Related information:

- [PXIe-7890/7891 Getting Started](#)

## Digital I/O

Number of channels	64
Signal type	Single-ended
<b>Voltage level</b>	
Digital input	3.3 V / 5 V (selectable by bank of 16 channels)
Digital output	3.3 V / 5 V (selectable by bank of 16 channels)
Direction control	Per channel
Latency	25 ns

Power-on-state	Digital input
Number of external clock input	2
Protection	±15 V per line, up to two lines simultaneously



**Note** Digital input and output voltage levels are guaranteed by design through the digital buffer specifications.

Table 5. Digital Input Logic Levels

Voltage Family	Input Low Voltage ( $V_{IL}$ ) Maximum	Input High Voltage ( $V_{IH}$ ) Minimum
3.3 V	0.80 V	2.00 V
5.0 V	1.50 V	3.50 V

Minimum input voltage	0 V
Maximum input voltage	5 V
Input impedance	100 k $\Omega$ , pull-down

Table 6. Digital Output Logic Levels

Voltage Family	Current	Output Low Voltage ( $V_{OL}$ ) Maximum	Output High Voltage ( $V_{OH}$ ) Minimum
3.3 V	100 $\mu$ A	0.10 V	3.20 V
	4 mA	0.45 V	2.85 V
5 V	100 $\mu$ A	0.10 V	4.90 V

Voltage Family	Current	Output Low Voltage (V <sub>OL</sub> ) Maximum	Output High Voltage (V <sub>OH</sub> ) Minimum
	4 mA	0.45 V	4.55 V

Maximum DC output current per channel	4.0 mA (sink or source)
Output impedance	50 $\Omega$ $\pm$ 20%
Maximum output toggle rate	10 MHz

## Connector 1

The following section describes the analog output characteristics accessible through CONNECTOR 1. For more information, including pinout descriptions, refer to ***PXIe-7890/7891 Getting Started*** content in the NI Product Documentation Center.

Connector type	68-pin VHDCI receptacle
----------------	-------------------------

## Analog Output

Output type	Single-ended, voltage output
Number of channels	16
Resolution	16 bits

Update latency
----------------

Uncalibrated	440 nsec
Calibrated	460 nsec

Analog latency	75 nsec
Maximum update rate	2 MS/s
INL	±0.5 LSB typical, ±2 LSB maximum
DNL	±0.5 LSB typical, ±1 LSB maximum

<b>Output range</b>	
Nominal	±10 V
Typical	±10.13 V
Minimum	±10.10 V

Output coupling	DC
Output impedance	0.3 Ω

Gain drift	5.5 ppm/°C
Offset drift	30 $\mu$ V/°C
Slew rate	20 V/ $\mu$ s
Noise (DC to 612 kHz)	70 $\mu$ Vrms
Current drive	$\pm$ 15 mA

Protection	Short circuit to ground
Crosstalk @100 kHz	-85 dB

<b>Overvoltage protection</b>	
Powered on	$\pm$ 15 V
Powered off	$\pm$ 10 V

Power-on output state	0 V
Power-on glitch	640 mV, decays to 0 V in 860 $\mu$ s

Power-off glitch	1.4 V, decays to 0 V in 200 $\mu$ s
Glitch during module reset	1.4 V, decays to 0 V in 200 $\mu$ s



**Note** The IO Socket\Clock 100 MHz is the primary clocking resource for analog output.



**Note** Total hardware latency is Update latency + Analog latency.

Table 7. Settling Time

Step Size	Accuracy	
	$\pm 10$ V	$\pm 16$ LSB
$\pm 10$ V	3.0 $\mu$ s	7.4 $\mu$ s

Table 8. Analog Output Calibrated Accuracy

Nominal Range	Condition	Gain Error (Percent of Reading)	Offset Error
$\pm 10$ V	Typical (25°C to $\pm 5$ °C)	$\pm 0.016\%$	$\pm 0.11$ mV
$\pm 10$ V	Maximum (0°C to 55°C)	$\pm 0.070\%$	1.79 mV

Table 9. Analog Output Uncalibrated Accuracy

Nominal Range	Condition	Gain Error (Percent of Reading)	Offset Error
$\pm 10$ V	Typical (25°C to $\pm 5$ °C)	$\pm 0.096\%$	$\pm 2.73$ mV
$\pm 10$ V	Maximum (0°C to 55°C)	$\pm 0.219\%$	$\pm 8.86$ mV



**Note** Uncalibrated accuracy in [Table 9. Analog Output Uncalibrated Accuracy](#) refers to the accuracy achieved when outputting in raw or unscaled modes where the calibration constants stored in the module are not applied

to the data. The gain error is relative to the typical output range of  $\pm 10.13$  V.

#### AO Absolute Accuracy Equation

$$AO\_AbsoluteAccuracy = (OutputValue) \cdot GainError + OffsetError + INLError \cdot OutputRange \cdot 2 / 2^{16 \text{ bits}}$$

The following example calculates the absolute full scale calibrated accuracy at  $25 \pm 5^\circ\text{C}$  on the 10 V range.

$$AO\_AbsoluteAccuracy = (10 \text{ V}) \cdot 0.016 \% + 0.11 \text{ mV} + \frac{0.5 \text{ LSB} \cdot (10.13 \text{ V}) \cdot 2}{2^{16 \text{ bits}}} = 1.865 \text{ mV}$$

## Connector 2

The following section describes the analog input characteristics accessible through CONNECTOR 2. For more information, including pinout descriptions, refer to **PXIe-7890/7891 Getting Started** content in the NI Product Documentation Center.

Connector type	68-pin VHDCI receptacle
----------------	-------------------------

## Analog Input

Number of channels	8
Input mode	Differential
Type of ADC	Successive approximation register (SAR)
Resolution	16 bits

Input ranges	$\pm 20\text{ V}$ , $\pm 10\text{ V}$ , $\pm 5\text{ V}$ , $\pm 2\text{ V}$ , $\pm 1\text{ V}$
--------------	--

<b>Conversion latency</b>	
Uncalibrated	480 nsec
Calibrated	480 nsec

<b>Analog latency</b>	
Range $\pm 20\text{ V}$	415 nsec
Ranges $\pm 10\text{ V}$ , $\pm 5\text{ V}$ , $\pm 2\text{ V}$	170 nsec
Range $\pm 1\text{ V}$	200 nsec

Maximum rate (per channel)	2 MS/s
----------------------------	--------

<b>Input impedance</b>	
<b>Powered on</b>	
Range $\pm 20\text{ V}$	1 M $\Omega$
Range $\pm 10\text{ V}$ , $\pm 5\text{ V}$ , $\pm 2\text{ V}$ , $\pm 1\text{ V}$	> 1 G $\Omega$

Powered off/overload	3.8 k $\Omega$
----------------------	----------------

Input coupling sampling	DC
Input bias current	$\pm 5$ nA
Input offset current	$\pm 5$ nA
INL	$\pm 6$ LSB typical, $\pm 12.7$ LSB maximum
DNL	$\pm 0.4$ LSB typical, $\pm 1$ LSB maximum

<b>CMRR, DC to 60 Hz</b>	
Range $\pm 20$ V	-48 dB
Ranges $\pm 10$ V, $\pm 5$ V, $\pm 2$ V, $\pm 1$ V	-80 dB

<b>Bandwidth</b>	
<b>Small signal</b>	
Range $\pm 20$ V	900 kHz
Ranges $\pm 10$ V, $\pm 5$ V, $\pm 2$ V	1600 kHz

Range $\pm 1$ V	1400 kHz
<b>Large signal</b>	
Ranges $\pm 20$ V, $\pm 10$ V	740 kHz
Ranges $\pm 5$ V, $\pm 2$ V, $\pm 1$ V	970 kHz

Crosstalk (100 kHz) into $50 \Omega$	-70 dB
--------------------------------------	--------

<b>Overvoltage protection</b>	
Powered on	$\pm 42 \text{ V}^2$
Powered off	$\pm 30 \text{ V}$



**Note** The IO Socket\Clock 100 MHz is the primary clocking resource for analog input.



**Note** Total hardware latency is Conversion latency + Analog latency.

Table 10. Analog Input Characteristics by Range

Specification	Nominal Range: $\pm 20 \text{ V}$	Nominal Range: $\pm 10 \text{ V}$	Nominal Range: $\pm 5 \text{ V}$	Nominal Range: $\pm 2 \text{ V}$	Nominal Range: $\pm 1 \text{ V}$
Input noise ( $\mu\text{Vrms}$ )	1600	670	340	140	80

- Only valid for fault on +/- input for 8 AI channels maximum. Degrades to +/-30 V for all 16 channels fault.

Specification	Nominal Range: $\pm 20$ V	Nominal Range: $\pm 10$ V	Nominal Range: $\pm 5$ V	Nominal Range: $\pm 2$ V	Nominal Range: $\pm 1$ V
Gain drift (ppm/ $^{\circ}$ C)	22.6	16.7	16.7	16.7	16.7
Offset drift ( $\mu$ V/ $^{\circ}$ C)	64.0	29.2	14.9	6.5	3.8
Typical input range, AI+ to AI- (V)	$\pm 20.62$	$\pm 10.22$	$\pm 5.11$	$\pm 2.04$	$\pm 1.02$
Minimum input range, AI+ to AI- (V)	$\pm 20.38$	$\pm 10.16$	$\pm 5.08$	$\pm 2.03$	$\pm 1.01$
Maximum Working Voltage (V) (Signal + Common Mode to Ground)	$\pm 22$	$\pm 13$	$\pm 10.5$	$\pm 9.0$	$\pm 8.5$

Table 11. Analog Input Calibrated Accuracy

Nominal Range	Condition	Gain Error (Percent of Reading)	Offset Error
$\pm 20$ V	Typical ( $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ )	$\pm 0.038\%$	$\pm 1.44$ mV
$\pm 20$ V	Maximum ( $0^{\circ}\text{C}$ to $55^{\circ}\text{C}$ )	$\pm 0.278\%$	$\pm 5.94$ mV
$\pm 10$ V	Typical ( $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ )	$\pm 0.032\%$	$\pm 0.71$ mV
$\pm 10$ V	Maximum ( $0^{\circ}\text{C}$ to $55^{\circ}\text{C}$ )	$\pm 0.215\%$	$\pm 2.04$ mV
$\pm 5$ V	Typical ( $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ )	$\pm 0.032\%$	$\pm 0.36$ mV
$\pm 5$ V	Maximum ( $0^{\circ}\text{C}$ to $55^{\circ}\text{C}$ )	$\pm 0.215\%$	$\pm 1.05$ mV
$\pm 2$ V	Typical ( $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ )	$\pm 0.032\%$	$\pm 0.15$ mV
$\pm 2$ V	Maximum ( $0^{\circ}\text{C}$ to $55^{\circ}\text{C}$ )	$\pm 0.215\%$	$\pm 0.47$ mV
$\pm 1$ V	Typical ( $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ )	$\pm 0.032\%$	$\pm 0.08$ mV
$\pm 1$ V	Maximum ( $0^{\circ}\text{C}$ to $55^{\circ}\text{C}$ )	$\pm 0.215\%$	$\pm 0.27$ mV

Table 12. Analog Input Uncalibrated Accuracy

Nominal Range	Condition	Gain Error (Percent of Reading)	Offset Error
$\pm 20$ V	Typical ( $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ )	$\pm 0.143\%$	$\pm 3.10$ mV
$\pm 20$ V	Maximum ( $0^{\circ}\text{C}$ to $55^{\circ}\text{C}$ )	$\pm 0.808\%$	$\pm 22.80$ mV
$\pm 10$ V	Typical ( $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ )	$\pm 0.139\%$	$\pm 0.98$ mV

Nominal Range	Condition	Gain Error (Percent of Reading)	Offset Error
±10 V	Maximum (0°C to 55°C)	±0.536%	±6.89 mV
±5 V	Typical (25°C ± 5°C)	±0.142%	±0.54 mV
±5 V	Maximum (0°C to 55°C)	±0.546%	±3.67 mV
±2 V	Typical (25°C ± 5°C)	±0.142%	±0.28 mV
±2 V	Maximum (0°C to 55°C)	±0.546%	±1.74 mV
±1 V	Typical (25°C ± 5°C)	±0.142%	±0.19 mV
±1 V	Maximum (0°C to 55°C)	±0.546%	±1.09 mV



**Note** Uncalibrated accuracy in [Table 12. Analog Input Uncalibrated Accuracy](#) refers to the accuracy achieved when acquiring in raw or unscaled modes where the calibration constants stored in the module are not applied to the data. The gain error is relative to the typical input range from [Table 10. Analog Input Characteristics by Range](#). For example, on the ±10 V nominal range, the gain error is relative to a full-scale value of ±10.22 V.

### AI Absolute Accuracy Equation

$$AI\_AbsoluteAccuracy = \left( Reading \right) \cdot GainError + OffsetError + INLErrror \cdot InputRange \cdot 2 / 2^{16 \text{ bits}} + Noise \cdot CoverageFactor / \sqrt{Number\_of\_reading}$$

The following example calculates the absolute full scale calibrated accuracy at 25 ± 5 °C on the 20 V range with 10,000 readings and 3σ coverage factor.

$$AI\_AbsoluteAccuracy = \left( 20 \text{ V} \right) \cdot 0.038 \% + 1.44 \text{ mV} + \frac{6 \text{ LSB} \cdot (20.62 \text{ V}) \cdot 2}{2^{16 \text{ bits}}} + \frac{(1600 \text{ } \mu\text{V}) \cdot 3}{\sqrt{10,000}} = 12.864 \text{ mV}$$

## Connector 3

The following sections describe the low-latency analog output characteristics accessible through CONNECTOR 3. For more information, including pinout descriptions, refer to **PXIe-7890/7891 Getting Started** content in the NI Product Documentation Center.

Connector type	68-pin VHDCI receptacle
----------------	-------------------------

## Low-Latency Analog Output

Output type	Single-ended, voltage output
Number of channels	16
Resolution	16 bits
Output range	$\pm 10\text{ V}, \pm 0.5\text{ V}^3$

Update latency	
Uncalibrated	148 nsec
Calibrated	168 nsec

Analog latency	50 nsec
Maximum update rate	4 MS/s
INL	$\pm 4$ LSB maximum

3. The PXIe-7890 supports 0.5 V range only on Ch<0..7>.

DNL	$\pm 1$ LSB maximum
Output coupling	DC
Output impedance	50 $\Omega$
Slew rate	320 V/ $\mu$ s
Current drive	$\pm 100$ mA
Crosstalk @100 kHz	-78 dB

Protection	Short circuit to ground
------------	-------------------------

<b>Overvoltage protection</b>	
Powered on	$\pm 32$ V <sup>4</sup>
Powered off	$\pm 20$ V

Power on state	0 V
----------------	-----

<b>Power on glitch</b>
------------------------

4. AO channel will shut down at fault voltage more than  $\pm 5$  V from configured AO output.

Dual range channel	1.3 V, decays to 0 V in 400 $\mu$ s
Single range channel	0.4 V, decays to 0 V in 80 ms

Power off glitch	
10 V range channels	4.6 V, decays to 0 V in 4 $\mu$ s
0.5 V range channels	0.25 V, decays to 0 V in 4 $\mu$ s

Settling time at Full Scale to 16 LSB	1.2 $\mu$ s
---------------------------------------	-------------



**Note** The IO Socket\Clock 100 MHz is the primary clocking resource for low-latency analog output.



**Note** Total hardware latency is Update latency + Analog latency.

Table 13. Low-Latency Analog Output Characteristics by Range

Specification	Nominal Range: $\pm 10$ V	Nominal Range: $\pm 0.5$ V
Output Noise ( $\mu$ Vrms) – DC to 612 kHz	78	16
Gain Drift (ppm/ $^{\circ}$ C)	13	78
Offset Drift ( $\mu$ V/ $^{\circ}$ C)	260	13
Typical Output Range (V)	$\pm 10.32$	$\pm 0.51$
Minimum Output Range (V)	$\pm 10.15$	$\pm 0.50$

Information in [Table 14. Low-Latency Analog Output Calibrated Accuracy](#) and [Table 15.](#)

Low-Latency Analog Output Uncalibrated Accuracy is applicable only for high impedance loads (> 1 Mohm), in which the load current is negligible due to the 50 ohm source resistance.

Table 14. Low-Latency Analog Output Calibrated Accuracy

Nominal Range	Condition	Gain Error (Percent of Reading)	Offset Error
±10 V	Typical (25°C to ±5°C)	±0.028%	±2.67 mV
±10 V	Maximum (0°C to 55°C)	±0.162%	±19.94 mV
±0.5 V	Typical (25°C to ±5°C)	±0.099%	±0.13 mV
±0.5 V	Maximum (0°C to 55°C)	±0.852%	±1.03 mV

Table 15. Low-Latency Analog Output Uncalibrated Accuracy

Nominal Range	Condition	Gain Error (Percent of Reading)	Offset Error
±10 V	Typical (25°C to ±5°C)	±0.256%	±24.42 mV
±10 V	Maximum (0°C to 55°C)	±0.828%	±81.65 mV
±0.5 V	Typical (25°C to ±5°C)	±1.164%	±1.22 mV
±0.5 V	Maximum (0°C to 55°C)	±4.319%	±4.21 mV



**Note** Uncalibrated accuracy refers to the accuracy achieved when outputting in raw or unscaled modes where the calibration constants stored in the module are not applied to the data. The gain error is relative to the typical output from [Table 13. Low-Latency Analog Output Characteristics by Range](#). For example, on the ±10 V nominal range, the gain error is relative to a full-scale value of ±10.32 V.

#### Low Latency AO Absolute Accuracy Equation

$$LLAO\_AbsoluteAccuracy = \left( OutputValue \right) \cdot GainError + OffsetError + INLError \cdot OutputRange \cdot 2 / 2^{16 \text{ bits}}$$

The following example calculates the absolute full scale calibrated accuracy at 25 ±5 °C on the 10 V range.

$$LLAO\_AbsoluteAccuracy = (10 \text{ V}) \cdot 0.028 \% + 2.67 \text{ mV} + \frac{4 \text{ LSB} \cdot (10.32 \text{ V}) \cdot 2}{2^{16} \text{ bits}} = 6.730 \text{ mV}$$

## Calibration

Interval	2 years
----------	---------

## Reconfigurable FPGA

The PXIe-7890 provides a KU060 FPGA with characteristics shown in the following table.

Table 16. KU060 FPGA Characteristics

Characteristics	KU060
LUTs	331,680
DSP48 slices (25 × 18 multiplier)	2,760
Embedded Block RAM	38.0 Mb
Timebase reference sources	PXI Express 100 MHz (PXIe_CLK100)
Data transfers	DMA, interrupts, programmed I/O, multi-gigabit transceivers
Number of DMA channels	60



**Note** The list above depicts the total number of FPGA resources available on the part. The number of resources available to the user is slightly lower, as some FPGA resources are consumed by board-interfacing IP for PCI Express, device configuration, and various board I/O. For more information, contact NI Support.

## Onboard DRAM

Memory size	4 GB (2 banks of 2 GB)
DRAM clock rate	1064 MHz
Physical bus width	32 bit
LabVIEW FPGA DRAM clock rate	267 MHz
LabVIEW FPGA DRAM bus width	256 bit per bank
Maximum theoretical data rate	17 GB/s (8.5 GB/s per bank)

## Bus Interface

Form factor	PCI Express Gen-3 x8
-------------	----------------------

## Maximum Power Requirements



**Note** Power requirements are dependent on the contents of the LabVIEW FPGA VI used in your application.

Maximum Current	
+3.3 Vdc	2.3 A

+12.0 Vdc	4.2 A
Maximum total power	58.0 W

Power consumption is from both PXI Express backplane power connectors.

## Physical Characteristics

Dimensions (not including connectors)	4.0 cm × 13.0 cm × 21.6 cm (0.8 in. × 5.1 in. × 8.5 in.)
Weight	771 g (27.2 oz)

## Environmental Characteristics

Table 17. Temperature

Operating	0 °C to 55 °C
Storage	-40 °C to 71 °C

Table 18. Humidity

Operating	10% to 90%, noncondensing
Storage	5% to 95%, noncondensing

Table 19. Pollution Degree

Pollution degree	2
------------------	---

Table 20. Maximum Altitude

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
------------------	---

Table 21. Shock and Vibration

Operating vibration	5 Hz to 500 Hz, 0.3 g RMS
Non-operating vibration	5 Hz to 500 Hz, 2.4 g RMS
Operating shock	30 g, half-sine, 11 ms pulse